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During the VLSI Digital Design course, the delegates will gain a thorough understanding of key aspects related to power management, clock requirements, synchronization, clock-gating and RTI coding considerations. Based on the training program, the delegates will build sound awareness on the fundamentals of IP MMR interfaces based on AMBA APB and AXI4-Lite protocols, design for Test and Manufacturing and Bus Protocols and typical side-band signals. The course enables the delegates to create simple test benches for simulating/debugging IP designs and systematically plan and implement the RTL.

The course introduces delegates to the commonly used Verilog/SystemVerilog constructs, progressive design implementation exercises, robust design techniques, Basic synthesis and gate-netlist schematic analysis exercises. After the completion of the VLSI Digital Design course, the delegates can use their experience and knowledge gained from the course in getting the competitive edge towards becoming a high-performing VLSI professional. The course also prepares delegates to perform confidently in job interviews.

During the Essentials of Professional VLSI Digital Design training program, the delegates will be introduced to the fundamentals of Digital Design, key aspects related to synchronization, timing and clock, IP/SOC design flows, power management techniques, Finite state machines and Power performance trade-offs. The course is beneficial for electronics engineering graduate students who are already familiar with the digital design. This certification helps them becoming self-sufficient with RTL coding with free EDA tools and also build their career with VLSI products.

Prerequisites

The delegates are expected to have:

- Bachelor’s degree in Electronics Engineering
- Understanding of Verilog RTL coding and UNIX basics
- Basic knowledge of fundamentals of digital design

Course Objectives

- Acquire a comprehensive knowledge of key aspects: Clock-gating, RTL coding considerations, Finite State Machines, Clock requirements, Power management
- Gain an understanding of SystemVerilog coding construct
- Lay strong foundation on Industry standard IP MMR interfaces based on AMBA APB and AXI4-Lite protocols, Design for Test and Manufacturing and Power-Performance-Area (PPA) trade-offs
- Understand Physical design flows, IP and SOC design cycles, Gate Netlist generation flows
- Learn how to operate in professional VLSI development environment

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- Key RTL Coding Considerations and Environment/Tool Familiarization
- Clock-gating and Synchronization, SystemVerilog Labs
- Resets, Bus Interfaces and Side-band Signals, SystemVerilog Labs
- Physical Design Flows and Semiconductor Manufacturing process - Overview, Synthesis Labs and Mini-Project1 start
- Essentials of Clocking, SystemVerilog Labs
- Power-Performance-Area (PPA) Trade-Offs, SystemVerilog Labs and Perl quick-start
- Design For Test and Manufacturability, SystemVerilog Labs and Perl quick-start
- Finite State Machines and Power Management Techniques, SystemVerilog Labs
- IP/SOC Design Flows and Gate-Netlist generation Flows - Overview, Synthesis Labs
- AMBA APB and AXI4-Lite Bus Interfaces, Mini-Project1 follow-on and Mini-Project2 start
- Pointers for further learning and Online resources, Review of the Mini-Projects

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